IN THE SPECIFICATION

Please delete the Title at page 1, lines 2-3, in its entirety and replace with the following new Title:

SEMICONDUCTOR DEVICE HAVING A HIGH-K METAL OXIDE AND SILICON OXIDE COMPOUND INSULATING FILM

Please insert the following heading on page 1, between lines 10-11:

FIELD OF THE INVENTION

Please insert the following heading on page 1, between lines 17-18:

DISCUSSION OF THE BACKGROUND

Please amend the heading on page 8, line 10 as follows:

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Please replace the paragraph at page 9, lines 21-24, with the following rewritten paragraph:

FIGS. 13A to 13C are cross sectional views collectively showing the basic structure of the semiconductor device according to ~~other~~ another embodiment of the present invention;

Please replace the paragraph at page 11, line 11, to page 12, line 4, with the following rewritten paragraph:

Whether or not the crystals within the thin film are nano-crystals ~~are~~ is determined as follows. Specifically, if an electron beam diffraction ED, in which the diameter of the beam is generally scores of nanometers, is applied to a sample to be measured, a spot-like diffraction

image is obtained in the case where the sample is a single crystal, and a ring-like diffraction image (polycrystalline ring) is obtained in the case where the sample is polycrystalline. It should be noted that, if the diameter of the electron beam is diminished to a nanometer order (1 nm to 10 nm), e.g., about 5 nm, the diffraction image forms a spot even in the case of the polycrystal, and a polycrystalline ring can be observed in the case of the microcrystal smaller than the polycrystal. It follows that, in the case of employing electron beam diffraction using an electron beam having a very small diameter of about 5 nm, it is possible to determine whether or not the sample to be measured is microcrystalline depending on whether or not the polycrystalline ring can be observed.

Please replace the paragraph at page 12, lines 11-22, with the following rewritten paragraph:

said insulating film containing a silicon compound containing at least one element selected from the group consisting of an oxygen and a nitrogen, and a metal compound containing a metal other than silicon and at least one element selected from the group consisting of an oxygen and a nitrogen, nano-crystals being formed in said insulating film, the size of said ~~nano-crystal~~ nano-crystals being small enough to permit observation of a polycrystalline ring as a diffraction image when an electron beam having a beam diameter of the nanometer order is incident in parallel to said insulating film surface.

Please replace the paragraph at page 13, lines 5-8, with the following rewritten paragraph:

The nano-crystals may be formed in the insulating film, it ~~is~~ then being preferable that the size of the largest nano-crystal grain in the insulating film ~~being~~ is not larger than the thickness of the insulating film.

Please replace the paragraph at page 19, line 20, to page 20, line 7, with the following rewritten paragraph:

Further, [[an]] As ions are implanted with a dose of 1×10^{14} cm^{-2} under an accelerating energy of 300 eV by using the SiGe film 24 as a mask, as shown in FIG. 4D. Then, a SiN film is deposited on the entire surface, followed by etching back the SiN film on the entire surface by RIE so as to form a gate side wall SiN film 25 in a thickness of 10 nm. Further, As ions are implanted again at a dose of 1×10^{15} cm^{-2} under an accelerating energy of 10 keV with the SiGe film 24 and the SiN film 25 used as a mask. Still further, an RTA (rapid temperature annealing) is applied at a temperature between 900°C and 1200°C for about 1 to 30 seconds so as to form source-drain regions 26a, 26b and to add an n-type impurity to the SiGe film 24 forming the gate electrode.

Please replace the paragraph at page 35, lines 2-21, with the following rewritten paragraph:

As described above, in the another embodiment of the present invention, the crystals precipitated in the gate insulating film formed of a highly dielectric film are not polycrystals but single crystals and are sufficiently smaller than the gate length Lg. Also, an amorphous material enters the crystal grain boundary. As a result, it is possible to suppress the leakage current derived from the crystal boundary. In addition, a plurality of nano-crystals are present in the longitudinal direction of the gate, and the size of the nano-crystal is substantially equal to the width W of the mixed film such that the crystal boundary extends through the front surface and the back surface of the film. It follows that it is possible to markedly decrease the trap density that is dependent on the energy level of the nano-crystal present in the mixed

film. In order to obtain a high dielectric constant, it is desirable for at least the nano-crystals of a metal oxide to be dispersed in the gate insulating film.

Please replace the paragraph at page 42, lines 11-22, with the following rewritten paragraph:

It is not absolutely necessary for the nano-crystals to extend across the insulating film. As shown in FIGS. 13B and 13C referred to previously, it is possible for a thin SiO_2 film to be formed between the edge portion of the nano-crystal and the surface of the mixed film. Even in this case, if the thickness of the SiO_2 film is not larger than 0.7 nm, the distance from the interface of the mixed film is not larger than 0.7 nm in most of the ~~microcrystals~~ nano-crystals because the grain diameter of the nano-crystal is sufficiently large. It follows that the inconvenience of the trapped electric charge is not generated.

Please replace the paragraph at page 48, lines 22-26, with the following rewritten paragraph:

The present invention is not limited to each of the Examples described above. These Examples can be employed singly or in combination. It is also possible to combine the Examples described above with the method described below.

Please replace the paragraph at page 52, line 25, to page 53, line 8, with the following rewritten paragraph:

Each of the Examples described above is directed to a MOS transistor. However, it is possible to apply the technical idea of the present invention to various semiconductor devices using a highly dielectric insulating film including, for example, a MOS capacitor. Further, as already described in conjunction with Example 1, the technical idea of the present invention

can be applied to a MOSFET of SOI structure and to a vertical MOS ~~devices~~ device. Further, various modifications are available within the technical scope of the present invention.